

CLAIMS

1. A microelectronic assembly, comprising:
 - a) a dielectric layer having an attachment portion, the dielectric layer having at least one offset portion offset from the attachment portion in a generally downward direction;
 - b) a semiconductor chip assembled to the attachment portion; and
 - c) terminal structures carried by the offset portion of the dielectric layer for connecting the semiconductor chip with external circuitry lying at a lower level than the attachment portion.
2. The assembly of claim 1, wherein the attachment portion of the dielectric layer is generally planar.
3. The assembly of claim 1, wherein the dielectric layer has at least one bend in the dielectric layer between the attachment portion and the offset portion.
4. The assembly of claim 3, wherein the at least one bend comprises a first bend in a first direction and a second bend in a second direction opposite to the first direction.
5. The assembly of claim 4, wherein the dielectric layer has at least one conductor extending in the bend.
6. The assembly of claim 5, wherein the at least one conductor is arranged so as to support the bend in the dielectric layer.
7. The assembly of claim 1, wherein the dielectric layer comprises a polymeric material molded so as to form the offset portion.
8. The assembly of claim 1, wherein the semiconductor chip is attached to the dielectric layer at a bottom surface of the dielectric layer and the offset portion of the dielectric layer extends generally downwardly alongside the semiconductor chip.

9. The assembly of claim 8, wherein the dielectric layer has at least one conductor, arranged so as to shield the semiconductor chip.

10. The assembly of claim 1, wherein the offset portion of the dielectric layer comprises a portion that lies underneath the attachment portion of the dielectric layer.

11. The assembly of claim 1, wherein the offset portion of the dielectric layer comprises a portion that lies outwardly of the attachment portion of the dielectric layer.

12. The assembly of claim 1, wherein the dielectric layer has at least one outer end and the terminal structures are disposed at the at least one outer end.

13. The assembly of claim 12, wherein the at least one outer end extends generally horizontally.

14. The assembly of claim 1, wherein the semiconductor chip comprises a first microelectronic element and further comprising a second microelectronic element, the first microelectronic element being disposed at a top surface of the dielectric layer and the second microelectronic element being disposed at a bottom surface of the dielectric layer.

15. The assembly of claim 14, wherein the dielectric layer comprises a first dielectric layer, and further comprising a second dielectric layer, the second microelectronic element being attached to the second dielectric layer and arranged so that the second microelectronic element overlies the first microelectronic element.

16. The assembly of claim 1, further comprising a circuit element connected to the terminal structures so that the circuit element is disposed underneath the dielectric layer.

17. The assembly of claim 16, wherein the terminal structures interconnect the semiconductor chip with the circuit element.

18. The assembly of claim 1, wherein the dielectric layer includes traces connected to the terminal structures and connected to contacts of the semiconductor chip.

19. The assembly of claim 1, wherein the semiconductor chip has a first face with contacts exposed at the first face.

20. The assembly of claim 19, wherein the semiconductor chip is assembled to the attachment portion so that the first face faces in an upward direction.

21. The assembly of claim 1, wherein the dielectric layer comprises a continuous sheet.

22. The assembly of claim 1, wherein the terminal structures comprise bonding material.

23. The assembly of claim 1, wherein the terminal structures are connected to conductors extending through the attachment portion.

24. The assembly of claim 1, wherein the terminal structures comprise solder balls.

25. A microelectronic assembly, comprising:

a) a dielectric layer having an attachment portion, the dielectric layer having outer ends lying outwardly of the attachment portion, the outer ends being offset from the attachment portion;

b) a semiconductor chip assembled to the attachment portion; and

c) terminal structures carried by the outer ends of the dielectric layer for connecting the semiconductor chip with external circuitry.

26. The assembly of claim 25 wherein the attachment portion of the dielectric layer is generally planar.

27. The assembly of claim 25, wherein the outer ends extend downwardly alongside the semiconductor chip and have at

least one conductor, arranged so as to shield the semiconductor chip.

28. The assembly of claim 25, wherein the dielectric layer has at least one bend in the dielectric layer between the attachment portion and the outer ends.

29. The assembly of claim 28, wherein the at least one bend comprises a first bend in a first direction and a second bend in a second direction opposite to the first direction.

30. The assembly of claim 28, wherein the dielectric layer has at least one conductor extending in the bend.

31. The assembly of claim 30, wherein the at least one conductor is arranged so as to support the bend in the dielectric layer.

32. The assembly of claim 25, wherein the semiconductor chip is attached to the dielectric layer at a bottom surface of the dielectric layer and the outer ends of the dielectric layer extend generally downwardly alongside the semiconductor chip.

33. The assembly of claim 25, wherein the outer ends of the dielectric layer extend generally horizontally.

34. The assembly of claim 25, wherein the outer ends lie underneath the attachment portion of the dielectric layer.

35. The assembly of claim 25, wherein the outer ends lie outwardly of the attachment portion of the dielectric layer.

36. The assembly of claim 25, wherein the semiconductor chip comprises a first microelectronic element and further comprising a second microelectronic element, the first microelectronic element being disposed at a top surface of the dielectric layer and the second microelectronic element being disposed at a bottom surface of the dielectric layer.

37. The assembly of claim 36, wherein the dielectric layer comprises a first dielectric layer and further comprising a second dielectric layer, the second microelectronic element

being attached to the second dielectric layer and arranged so that the second microelectronic element overlies the first microelectronic element.

38. The assembly of claim 25, further comprising a circuit element connected to the terminal structures so that the circuit element is disposed underneath the dielectric layer.

39. The assembly of claim 38, wherein the terminal structures interconnect the semiconductor chip with the circuit element.

40. The assembly of claim 25, wherein the dielectric layer includes traces connected to the terminal structures and connected to contacts of the semiconductor chip.

41. The assembly of claim 25, wherein the semiconductor chip has a first face and contacts exposed at the first face.

42. The assembly of claim 41, wherein the semiconductor chip is assembled to the attachment portion so that the first face faces in an upward direction.

43. The assembly of claim 25, wherein the dielectric layer comprises a continuous sheet.

44. The assembly of claim 25, wherein the terminal structures comprise bonding material.

45. The assembly of claim 25, wherein the terminal structures are connected to conductors extending through the attachment portion.

46. The assembly of claim 25, wherein the terminal structures comprise solder balls.

47. A microelectronic component, comprising:

a) a dielectric layer comprising a continuous sheet having an attachment portion for assembly with a microelectronic element and an offset portion offset from the attachment portion;

b) terminal structures on the dielectric layer; and

c) conductors attached to the terminal structures.

48. The component of claim 47, wherein the terminal structures include bonding material.

49. The component of claim 47, wherein the dielectric layer includes at least one bend between the attachment portion and the offset portion.

50. The component of claim 47, wherein the at least one bend comprises a first bend in a first direction and a second bend in a second direction opposite the first direction.

51. The component of claim 47, wherein the conductors comprise a plurality of traces.

52. The component of claim 51, wherein at least one of the traces is disposed in the bend.

53. The component of claim 47, wherein the attachment portion is generally horizontal and the offset portion generally extends downwardly.

54. The component of claim 47, wherein the offset portion lies outwardly of the attachment portion.

55. The component of claim 47, wherein the offset portion lies underneath the attachment portion.

56. The component of claim 47, wherein the dielectric layer comprises a polymeric material molded so as to form the offset portion.

57. The component of claim 47, wherein the terminal structures include vias defined by the dielectric layer.

58. The component of claim 47, wherein the terminal structures comprise bonding materials.

59. The component of claim 47, wherein the terminal structures comprise solder balls.